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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,149	10/31/2006	Lay-Lay Chua	Q95891	5622
23373	7590	04/30/2008	EXAMINER	
SUGHRUE MION, PLLC			JAHAN, BILKIS	
2100 PENNSYLVANIA AVENUE, N.W.				
SUITE 800			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20037			2814	
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			04/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,149	CHUA ET AL.	
	Examiner	Art Unit	
	BILKIS JAHAN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-21 is/are pending in the application.
 - 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) ____ is/are allowed.
- 6) Claim(s) 1-21 is/are rejected.
- 7) Claim(s) ____ is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 July 2006 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>7/14/06</u> . | 6) <input type="checkbox"/> Other: ____ . |

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-15, 17-19, 20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1+2, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 3, 6, 6, 1+2, respectively of U.S. Patent No. US 2007/0278478 A1. Although the conflicting claims are not identical, they are not patentably distinct from each other because the concept of claims 1-15, 17-19, 20 are same of the claims 1+2, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 3, 6, 6, 1+2, in the U.S. Patent No. US 2007/0278478 A1.

Regarding claims 16 and 21, U.S. Patent No. US 2007/0278478 A1 discloses all the limitations of claims 1-15 above. Therefore, these claims limitations are already covered above.

This is a double patenting rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaumseil et al (US 2007/0278478 A1).

Regarding claim 1, Zaumseil et al disclose an n-channel or ambipolar field-effect transistor (claim 2) including

- an organic semiconductive layer having an electron affinity EAsemicond (claim 1, line 2); and
- an organic gate dielectric layer (claim 1, line 3) forming an interface with the semiconductive layer (claim 1, line 4); characterized in that the bulk

concentration of trapping groups in the gate dielectric layer is less than 10^{18}cm^{-3}
(claim 1, lines 5-6), where

- a trapping group is a group having (i) an electron affinity EA_x greater than or equal to EA_{semicond} and/or (ii) a reactive electron affinity EA_r_{xm} greater than or equal to (EA_{semicond}.-2eV) (claim 1, lines 7-9).

Regarding claim 2, Zaumseil et al disclose a transistor according to claim I,
wherein the transistor is an ambipolar field-effect transistor (claim 2).

Regarding claim 3, Zaumseil et al disclose a transistor according to any one of the preceding claims wherein EA_{semicond} is greater than or equal to 2eV (claim 3).

Regarding claim 4, Zaumseil et al disclose a transistor according to claim 3 wherein EA_{semicond} is in the range of from 2eV to 4eV (claim 4).

Regarding claim 5, Zaumseil et al disclose a transistor according to any one of the preceding claims wherein the gate dielectric layer comprises an organic insulating material and the organic insulating material does not contain a repeat unit or residue unit comprising a trapping group (claim 5).

Regarding claim 6, Zaumseil et al disclose a transistor according to any one of the preceding claims, wherein the insulating material does not contain a repeat unit or

residue unit comprising a group having (i) an electron affinity EAx greater than or equal to 3eV and/or (ii) a reactive electron affinity EArxn greater than or equal to 0.5eV (claim 6).

Regarding claim 7, Zaumseil et al disclose a transistor according to claim 6 wherein the insulating material does not contain a repeat unit or residue unit comprising a quinone, aromatic -OH, aliphatic - COOH, aromatic -SH, or aromatic -COOH group (claim 7).

Regarding claim 8, Zaumseil et al disclose a transistor according to any one of the preceding claims, wherein the insulating material contains one or more groups selected from alkene, alkylene, cycloalkene, cycloalkylene, siloxane, ether oxygen, alkyl, cycloalkyl, phenyl, and phenylene groups (claim 8).

Regarding claim 9, Zaumseil et al disclose a transistor according to any one of claims 5 to 8 wherein the insulating material comprises an insulating polymer (claim 9).

Regarding claim 10, Zaumseil et al disclose a transistor according to claim 9, wherein the insulating polymer is selected "from the group consisting of substituted and unsubstituted poly(siloxanes) and copolymers thereof; substituted and unsubstituted poly(alkenes) and copolymers thereof; substituted and unsubstituted poly(styrenes) and

copolymers thereof; and substituted and unsubstituted poly(oxyalkylenes) and copolymers thereof (claim 10).

Regarding claim 11, Zaumseil et al disclose a transistor according to claim i0, wherein the backbone of the insulating polymer comprises a repeat unit comprising - Si(R)₂-O-Si(R)₂- where each R independently is methyl or substituted or unsubstituted phenyl (claim 11).

Regarding claim 12, Zaumseil et al disclose a transistor according to any one of claims 9 to ii, wherein the insulating polymer is crosslinked (claim 12).

Regarding claim 13, Zaumseil et al disclose a transistor according to any one of the preceding claims wherein the organic semiconductive layer comprises a semiconductive polymer (claim 13).

Regarding claim 14, Zaumseil et al disclose a transistor according to any one of claims 1 to 12 wherein the organic semiconductive layer comprises a semiconductive oligomer (claim 14).

Regarding claim 15, Zaumseil et al disclose a transistor according to any one of claims 1 to 12 wherein the organic semiconductive layer comprises a semiconductive small molecule (claim 15).

Regarding claims 16 and 21, Zaumseil et al disclose a method for making a transistor as defined any one of claims 1 to 15 (claims 1-15 covered all limitations above. Therefore, these claim limitations are already covered above).

Regarding claim 17, Zaumseil et al disclose Use of a transistor according to any one of claims 1 to 15 for n-channel conduction in an n-chanonel or ambipolar field effect transistor (claim 3).

Regarding claim 18, Zaumseil et al disclose Use of an organic gate insulating material that does not contain any chemical groups having (i)EAx greater than or equal to 3eV and/or (ii)EAzxn greater than or equal to 0.5eV, for n-channel conduction (claim 6).

Regarding claim 19, Zaumseil et al disclose a Use according to claim 18, wherein the insulating material does not contain any chemical groups having (i)EAx greater than or equal to 2eV and/or (EAx) greater than or equal to 0eV (claim 6).

Regarding claim 20, Zaumseil et al disclose a circuit, complementary circuit, or logic circuit including a transistor as defined in any one of claims 1 to 15 (claim 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BILKIS JAHAN whose telephone number is (571)270-5022. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

BJ